1. (Amended) A method for forming a semiconductor device, comprising:

etching a first portion of a dielectric layer formed on a semiconductor topography with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen and comprises C_4F_8; and

etching a second portion of the dielectric layer with a second etch chemistry different from the first etch chemistry.

5. (Amended) The method of claim 1, wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of a gate structure formed adjacent to the second portion.

7. (Amended) The method of claim 1, wherein the first etch chemistry further comprises CO.

11. (Amended) The method of claim 1, further comprising forming said dielectric layer on said semiconductor topography in one processing step.

12. (Amended) The method of claim 1, wherein the first etch chemistry has a dielectric material:silicon nitride selectivity of at least approximately 10:1, and wherein the dielectric layer comprises the dielectric material.

13. (Amended) The method of claim 1, wherein the second etch chemistry has a dielectric material:silicon oxide selectivity of at least approximately 5:1, and wherein the dielectric layer comprises the dielectric material.

17. (Amended) A method for forming a contact hole, comprising:

depositing a dielectric layer upon first and second gate laterally spaced gate structures on a semiconductor layer comprising isolation regions;

etching a first portion of the dielectric layer with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen; and

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etching a second portion of the dielectric layer with a second etch chemistry, wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of the first and second gate structures.

19. (Amended) The method of claim 17, wherein the dielectric layer comprises a doped silicon oxide having a phosphorus concentration of less than approximately 6 wt.%.

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20. (Amended) The method of claim 17, wherein etching the first portion of the dielectric layer exposes upper corners of the first and second gate structures, and wherein etching the second portion of the dielectric layer exposes the semiconductor layer.

Please add the following claims:

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22. (Added) The method of claim 17, wherein the dielectric layer is substantially continuous.

23. (Added) The method of claim 17, wherein the second etch chemistry comprises $C_2H_2F_4$.

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24. (Added) The method of claim 17, wherein the dielectric layer is in contact with a sidewall spacer of the first and second gate structures and the semiconductor layer.

25. (Added) The method of claim 17, wherein the first etch chemistry has a dielectric material:silicon nitride selectivity of at least approximately 10:1, and wherein the dielectric layer comprises the dielectric material.

26. (Added) The method of claim 17, wherein the second etch chemistry has a dielectric material:silicon oxide selectivity of at least approximately 5:1, and wherein the dielectric layer comprises the dielectric material.